MODELING AND OPTIMIZATION
FOR DEFECT-TOLERANT
NANO COMPUTER SYSTEM

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CHAPTER 1

INTRODUCTION

Reliability and yield assurance is one of the most emphasized requirements in nano-scale computing circuits and systems design as defects and faults due to harsh environment in the nano-scale geometry can be experienced throughout the manufacturing process [9], [10]. Efforts have been made to achieve acceptable reliability for these devices by employing conventional redundancy or repair-based approaches as practiced in design and manufacturing of CMOS-based circuits and systems. Among various defect and fault-tolerance techniques available for nano-scale systems designs, employing redundancy is the most common for the enhancement of reliability under defects and faults [10], [5], [11], [9], [16].

In order to efficiently and effectively model and evaluate the expected reliability of a fault-tolerant nano-scale circuits and systems, the defects and faults unique to the nano-scale devices under investigation must be identified, which may dictate substantially different defect and fault tolerance techniques from the conventional ones, thereby requiring new modeling and evaluation methods for reliability assurance. It has been reported that NW exhibits several types of defects depending on how a NW gets defective during the manufacturing process [9], [10], [5]. Broken NW is the primary cause of the defects [8]. The attempts to assess and predict the reliability of NW-based circuits and systems with broken NW-caused defects have
mainly employed the reliability or yield model with an assumption of compound binomial distribution of defects [10], [5], [9]. In this model, the nano-arrays are modeled as a fabric of rows and columns of NWs; and within each NW, the number of defects is assumed to follow binomial distribution. This model is based on the area-characteristic of the defects as different defects impact on different area in the NW. It is assumed that in the area-based models, defects occur dependently in the same NW, while occurrences of defects in different NWs are independent [10], [5], [9].

Programmable Nano-scale array in NASIC [15] (i.e., Nano-scale Application-Specific IC) may experience excessive interference and defects due to the harsh manufacturing environment [5]. In order to mitigate such noise and defects on the circuits, the nano arrays proposed in [17] employ PLA architecture, and utilize two levels of active redundancy, and faulty or malfunctioning columns or rows of NW in the array are replaced by using redundant NW. Another approach to tolerate such defects is replicating NWs in order to provide several alternative and detoured routing paths when defects occur [9]. In order for the above mentioned approaches to be able to provide defect tolerance, such costly steps as defect map extraction by utilizing reconfigurable devices; complex nano-micro interfacing-decoder required to address each crosspoint in the nano-fabric. Also, note that the above approaches are not readily realizable in nano-scale circuits and systems since they have been devised for very small defect rates in conventional micro CMOS circuits and systems [4], [16]. In [8], three defect tolerant techniques have been proposed in order to overcome above-mentioned limits, and they can address the defect and fault tolerance issues specific to nano-scale fabric-based circuits and systems [16]. An efficient and effective method to model and evaluate the effect of those proposed defect and fault tolerant techniques is a key to the success of deployment of reliable nano-fabric-based products under
such defects as broken NW. In [8], the effects of the proposed defect and fault
tolerance techniques have been demonstrated. However, they did not provide the
specific models they used to simulate how each technique affects the yield and how
combined techniques synergistically improve the yield. In this thesis, the synergetic
yield will be investigated as well as individual yield and reliability assessment.

The objective of this thesis is to develop a method to model and evaluate the
reliability of a defect tolerant NASIC under broken NW, and further provide a
guideline how to synergistically improve the yield and reliability with more accurate
prediction. Thereby, the more reliable nano-scale architecture can be realized with
respect to some elements while maintaining optimal requirements. This thesis is
organized as follows: In the next section, an overview of nanoelectronics, NASICs
and the architecture of the WISP-0 processor will be given. In Section 3, the various
defects and defect tolerant techniques proposed in [8] are introduced as the basis of
the reliability models to be proposed in this thesis. The proposed models to assure
reliability of the NASIC are developed in Sections 4. Parametric simulations and the
results are given in Section 5. Discussion and conclusions are given in the final
section.
Fundamental physical constraints in conventional electronics and the economics in the field are forecast to be forced to limit the continued advancement of the current state-of-the-art electronic devices manufactured by conventional fabrication and implementation methods and technologies in the next one or two decades [20]. Thus, it is exigently dictated to look for alternative methods and technology to fulfill the expected future computing demands. In nanoelectronics [17], the functional electronic structures are assembled with the well-defined nano-scale building blocks, such as carbon nanotubes (NTs), molecules, AND/OR semiconductor nanowires (NWs), and they are believed to the alternative solution to overcome the limits of the conventional technology [17]. NWs and NTs have been investigated for the use as building blocks for assembling various nano-devices such as FETs, p-n diodes, bipolar junction transistors, and complementary inverters, to mention a few [17], [21], [22], [10]. It has been reported that semiconductor nano-wire (NW)-based devices can be assembled in a predictable manner as the electronic properties and sizes of the NWs can be efficiently and effectively controlled during synthesis for parallel assembly [17]. Control of the assembly process of NW-based devices can be performed by using various forms of gates or diode junctions [5]. Also, it has been reported that using metallic gates [10], [2] and crossing NWs [17] can realize FET [14]. Crossing
NWs can be realized by varying the amount of oxide grown at the intersection, and a NW forms a diode with others, or behaves as a FET gate to the others, or they may disconnect [21], [22], [17]. The p-doped horizontal NWs and n-doped vertical NWs can form a nano-array. At the junctions of NWs, p-n diodes or FETs can be produced. Fluidic alignment, which involves suspending NWs in a solution (e.g., ethanol) and then making the fluid flow along precut channels on a surface, enables to build the arrays [5].

In this thesis, the defects and defect tolerance techniques for Nano-scale Application-Specific IC (NASIC) are considered as the basis of the proposed reliability modeling and its assurance. There has been few works that adequately addressed and resolved the yield and reliability issues in nanoelectronic devices. Also, not much have been achieved on innovations at systems level to study how to construct circuits and systems with such nanoelectronic devices. It is highly demanded to research on nano-scale computing systems as ITRS indicates that CMOS will reach its physical limit at 30nm or so in 10 years [12]. In this context, an alternative nano-scale systems technology and devices to replace the 30nm CMOS technology is to be exigently sought.

One of the most promising nanodevice technologies, such as arrays of semiconductor nanowires (NWs) and arrays of crossbar carbon nanotubes (NTs), can be used to realize FET and diode such that two crossing NWs with different doping types enable the voltage of one nanowire affect the conductance of the other, which works exactly the same way as the transistors in CMOS technology. The progresses made in the field, investigations on nano-scale computing systems at systems level are highly demanded and being extensively conducted.

NASICs are a tile-based architecture to build 2-D nano-fabrics as shown in Figure (1).
In general, programmable fabrics (e.g., nanofabrics) can offer programmability in a hierarchical manner, and provide a fast and flexibility prototyping capability in the application-specific domain. In regard of density that is one of the main motivations of nanoelectronic-based devices in the transition from the conventional micron-CMOS technology, nanoelectronic-based devices and design methods have an inherent density advantage over MOS [15], and NASIC also exploits the advantage. Moreover, fabrication constraints and fault-tolerance factors are taken into account the requirement for high density is more addressed [5].

NASIC design is based on a programmable grid-structure of CNTs and NWs [3], [4]. Each grid junction can be programmed either as a FET or a p-n type diode, or can also be disconnected in order to program and construct a hierarchical NASIC structure. Both FETs and diodes have been built and demonstrated based on NWs [10], [17] and CNTs [10]. At the grid junction, NASIC has a distinguishable characteristics compared to conventional PLA, such as doping of nano-grid strips, size of the NASIC tiles, and the use of specific sub-lithographic wires such as interconnect between tiles and the micro-level nanowires (MWs) [15].

Nanotile is the basic building block of NASICs. Each nanotile can implement a specific function such as adder, multiplexer and etc. as well as the NASIC-custom functions. The internal structure is a nano-array made of crossed nanowires. Horizontal nanowires are doped as p-type and vertical as n-type. A nanoarray is surrounded by microwires (MWs) which are used to drive nanowires and provide $vdd$(signals), and $gnd$(power supply). To program each NW junction, the number of MWs has to be at least logarithmic to the number of NWs [3], [4]. Pull up/down networks act as the interface between MWs and NWs and facilitate the addressing to every single nanowire.
Due to topological and doping constraints, latches or registers are difficult to implement on nanoarrays [5].

In case of NASICs, it is operated by 2-level $AND-OR$ logic planes in order to realize more efficient routing in a cascaded manner. As shown in Figure (2), the flip-flop has poor area efficiency for feedback network and it requires two doping types in horizontal or vertical dimension [15]. Moreover, large portion of the circuit perpendicular to the diagonal, so-called the diagonal effect, as defined by the $AND-NOR$ and $OR-NOR$ planes, cannot be utilized for active devices, because unlike in
Figure 2. An adder and a flip-flop (pull up/down are not shown) [15].

PLAs, it is impossible to provide ground lines (gnd) interleaved with the nanowires (for pull-down evaluation) [15], which impacts on the area efficiency negatively since these parts will be all wasted. A better way to implement sequential circuits to sustain the density advantage of nanoarray was proposed in [5].

As shown in Figure (3), instead of using static pull-up and pull-down arrays, dynamic precharge-evaluate transistors are inserted between vdd, gnd and nanoarray. A dynamic circuit which requires only one type of doping in each dimension provides a much better density compared to the static NASIC designs [5]. Pre signal enables writes and Eva signal enables reads. With the precharge-evaluate-hold phase, the data can be stored in nanowires temporarily, which is called the nano-latch [5].

Figure (4) shows a NASIC structure that is built by using pipelined dynamic nanotiles without latching the signals [5]. As a nano-latch is built on nanowires without requiring extra devices, it achieves a high density considerably. A nanotile
implemented by using the dynamic circuits is shown Figure (5).

Figure 3. Dynamic circuit and signal waveform [5].

Figure 4. Dynamic NASIC tile and Pipeline [5].
In order to investigate on the NASIC circuits particularly for yield-optimization purpose, the *wire streaming processors*, so-called WISP-0, is considered in this thesis. WISP-0 is a streaming processor with a 5-stage pipelining architecture [14]. It is a processor that the signals are streamed in and out through the nanowires. It consists of 5 nanotiles, as shown in Figure (6), in which each box surrounded by the dashed lines represents a nanotile. All adjacent nanotiles are connected by a set of NWs and each nanotile is driven by the surrounding MWs which carry ground, power supply voltage, and some control signals [13]. These nanotiles are all designed in a dynamic manner and are cascaded along on the wire to realize a 5-stage pipeline. The program counter out of 5-stage increases the instruction address in each cycle and the address fetches one instruction from instruction ROM and the instruction is decoded in the decoder unit. The decoded instruction enters Register File to read operands and ALU executes the operation. The final results are written back to Register File as shown in Figure (6) and (7).
The streaming processor architecture achieves the density advantage maximally and minimizes the loss due to manufacturing and device constraints when building nanoscale systems [14]. In this thesis, the yield of WISP-0 will be modeled an evaluated for optimization of the defect tolerance techniques in question.
CHAPTER 3

DEFECT TOLERANCE TECHNIQUES

The expected defects and failures in NW will be introduced and three defect tolerant techniques as proposed in [8] will be investigated. Those three defect tolerance techniques are based on the built-in redundancy, interleaving, and inserting weak pull-up/down NW [8].

As a unit circuit of interest, a single core NW array with \( n \) NW and 8 global interconnect microwires(MW) is considered in this chapter. In order to model the yield of a single element array effectively, the different defect factors are considered in this thesis as introduced in [16] and are shown in Figure (8). The following assumptions are made for the modeling purpose:

- **crosspoint failure** [10] – occurs with probability \( P_{CP} \); the contact between NW in a core nano array failed.

- **decoder pattern defect** [10] – occurs with probability \( P_{D} \); the failure during the decoder pattern programming on the array during directed self-assembly.

- **length defect** [10] – occurs with probability \( P_{L} \); a break or short in the NW at the junction.

Above defects have been reported [10] to occur in NW and they can effectively influence the yield. This physical phenomenon is referred to as *broken nanowire* [16].
Based on the possible defects, several nanofabric-based defect tolerant techniques have been introduced [8]. Those techniques are primarily centered around the reprogrammable crosspoints in a nanofabric such that it is required to access crosspoints in the nanofabrics for reconfiguration to achieve defect tolerance [16].

The interface between the micro and the nano-devices is required to provide alignment between NWs and MWs, which is one of the most challenging manufacturing issue [13]. An approach to address and resolve the issue is the CMOL, 

> **CMOS + MOLecular devices**, [7]. Other approaches use such methods as extracting defect maps, reconfiguration by utilizing reconfigurable devices [8].

Due to substantial difference of the circuit structure and physical constraints, the conventional yield models can not efficiently and effectively evaluate the yield of such nano circuits and systems with new defect tolerant techniques [9]. As in
general and practice, the circuits employ redundant NWs along with reprogrammability in order to tolerate the various kinds of defects [13]. The defect tolerant techniques specifically in WISP-0 processor under investigation for the yield modeling are: circuit-level built-in redundancy; NW interleaving; and inserting weak pull-up/down NWs [8].

3.1 Built-in Redundancy

Figure (9) shows a NASIC circuit which apply the built-in redundancy technique. Each vertical and horizontal NWs is implemented by sequential process of charging and evaluating in terms that horizontal NW is predischarged to “0” and vertical NW is precharged to “1”, respectively, then evaluated [16]. These flow makes the output to be \( o = ab + c \) in Figure (9). In most cases, the faulty signal “0” is masked by OR logic and “1” is masked by AND logic, respectively.

As scattered in nanotile, the defect signal can be masked through logic flow; signal masking is accomplished on a subsequent plane such that most signals can be calculated at next stage logic. For example, a fault on a vertical NW in the AND plane (see the position “A” in Figure (9)) make the NW to be faulty signal “0” due to disconnect with \( gnd \), a part of MW [8]. This faulty signal can be masked by following OR plane where exists in left side in Figure (9). Defect position “B” makes the whole NW to be a faulty signal “1” due to disconnect with \( vdd \) which is a part of MW [8]. It also can be masked by following AND plane where exist in right side in Figure (9). Similarly, the defect on horizontal NW in the AND plane (see the position “D” in Figure(9)) make the NW to be a faulty signal “1” because the horizontal NW is disconnected with \( gnd \) [13]. This fault can be masked by subsequent AND plane. Even if this masking mechanism tolerates most of the defect areas in nanotiles, it is
impossible to tolerate in some specific areas [13]. Break position “C” also make the whole NW to be a faulty signal “1” because it is disconnected with gnd [8]. However, there is no possible masking logic plane in current NW flow because next two vertical NWs in AND plane make the whole NW set to signal “1” after precharging. We called this area hard-to-mask [8].

Figure 9. An example of defect-tolerant circuit. “A”, “B” and “C” indicate different break positions on a horizontal NW [8]

3.2 Interleaving Nanowires

Interleaving nanowire handles the defect on middle of NW as well as mitigate the hard to mask area on built-in redundancy technique. In Figure (9), defect occurred in “C” is also to be hard to mask area; note again that all masking mechanism operates as sequential flow and converts faulty signal to normal in order to obtain desired operation. The fault signal makes the whole NW to be defective regardless of the number of crossed NW. The tolerant of this defect is accomplished by the interleaving. Interleaving technique compares the defective length on horizontal NW (note that
NW has its duplicated one in parallel manner. After the defective area is determined to be able to minimize, the defect length is converted to minimize in terms of switching NW [16].

In Figure (10), the operation of the proposed interleaving nanowire is given as follows: for two incoming elements o1 and o2 (with o1’ and o2’, respectively), the defective area of input with duplicated of each are checked first whether it can be reducible or not and then defect area of these four incoming elements are compared; if defect occurs on straddled part from o1’ to gnd, the input is switched from o1, o1’, o2, o2’ to o1, o2, o1’, o2’ [8]. The final output is issued from o1 and o2 except o2’ and o1’. Even if one of duplicated NW is defective, the whole process would make reliable result since the other one is issued to obtain correct output.

![Diagram](image)

Figure 10. Interleaving minimize the hard-to-mask area [13].

3.3 Inserting Weak Pull-up/down Nanowires

Although built-in redundancy and careful interleaving is performed, there still remains hard-to-mask lengths (logY) which is the length o2’ in Figure (10). A possible solution to solve this problem is to insert weak pull-down vertical NWs between the AND and OR planes [8] in terms that weak vertical NW play a role on
forcing the faulty signal “1” which is derived from defect position “C” to down signal “0” in order to be masked by AND plane [13]. Through this method, we can increase the yield of defect tolerance systems maximally. Similarly, weak horizontal NW is used to forcing the fault signal “1” which origin from defect position “E” in Figure (9) on AND plane to up into signal “1” in order to be masked by subsequent AND plane located in next subsequent nanotiles [13].

Figure 11. Adding weak pull-up/down NWs between OR and AND plane is helpful to decrease the defect area [8].
CHAPTER 4

MODELING AND YIELD ANALYSIS

4.1 Modeling Yield with No Defect Tolerance

In this section, the yield with no defect tolerance, that is raw yield, in NASIC with broken NWs is modeled. In order to measure the yield of non defect tolerant in NASIC architecture, a single NW in NASIC architecture is considered. The expected yield of a single NW, referred to as $P_{wire}$, is as follows.

$$P_{wire} = (1 - P_{CP})^{CP} \times (1 - P_l)^L \times (1 - P_D)^D$$

(4.1)

where,

- $L$: length of a nanowire in a nanotile
- $CP$: number of cross contacts of nanowires in a nanotile.
- $D$: number of decoders in a nanotile.
- $l$: defective nanowire length.
- $P_{CP}$: probability to be defective NW due to cross contact
- $P_l$: probability to be defective NW due to length
- $P_D$: probability to be defective NW due to decoder

$P_{wire}$ models the yield of a NW in the nanotile shown in Figure (8). A row of NW in
the nanotile consists of AND and OR logic to connect to a column of NW; connects the pull-down/up decoder blocks; and then connects to a microscale interconnect wire (i.e., a MW). Thus, the yield of a single nanowire, $P_{wire}$, has to take all related defects/failures into account. From Figure (8), the specific related yield parameters are the number of crosspoints (e.g., $CP = 10$), and the number of decoders (e.g., $D=2$), and the length of the defective nanowire (e.g., $l$). If defects hit on crosspoints, the $l$ is the length or distance from the crosspoint to the MW on the right end. If defects hit on the pull up/down decoders, the $l$ is the distance from the pull up/down decoder to the MW on the right end. It is assumed that each defect occurs following the binomial distribution dependently on each other if they are on the same NW while it is assumed the $n \times n$ nonowires on a nanotile occur independently. Each of those defects is referred to as the broken NW. It is reported that the broken NW defect is largely affected by the defect length ($l$) [12]. Therefore, $P_{wire}$ is determined by three different kinds of defects depending on how far the distances or lengths from the defect positions to each device of concern area; and can be modeled by considering the area-based structure.

Then, in order to extend the yield model of a NW to multiple NWs in which a certain number of NWs are being utilized as a quorum out of $n$ number of available NWs in each direction in the nanotile, it is to be checked how many NWs are addressed from $n$ number of column NWs and $n$ number of row NWs, respectively [6]. The yield of a row NW, $Y_{row}$, can be expressed as follows.

$$Y_{row} = \sum_{i=0}^{n} C(n, i) \times P_{wire}^{i} \times (1 - P_{wire})^{n-i} \quad (4.2)$$

where, $C(n, i)$ is the number of combinations of choosing $i$ column NWs out of $n$. 

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Based on the yield of row NWs in one nanotile, we can extend it to the yield of a single nanotile, by considering the yields of row and column NWs together as a series product under the assumption of independency between the defects on each NW. In the yield of row NWs, the selected row NWs can cross with column NWs chosen from $n$ number of column NWs in one nanotile. Then, we can calculate the yield of a nanotile. The net yield, referred to as $Y_{net}$, is the yield in which both the yield of the column and row NWs are taken together into account for the yield of a nanotile. The net yield can be expressed as follows.

$$Y_{net} = \sum_{i=0}^{n} \sum_{j=0}^{n} C(n,i) \times C(n,j) \times P_{wire}^{ij} \times (1 - P_{wire}^{ij})^{n^2 - ij}$$  \hspace{1cm} (4.3)$$

where,

• $i$: number of column nanowires chosen out of $n$ in a nanotile.

• $j$: number of row nanowires chosen out of $n$ in a nanotile.

• $n$: number of row/column nanowires in a NASIC.

• $ij$: $i \times j$.

4.2 Modeling Yield with Defect Tolerance

In this section, the yield with defect tolerance in a NASIC with broken NWs is modeled. The yield is modeled for three different defect tolerance techniques [16] as introduced in the previous chapter.

4.2.1 Built-in Redundancy

The yield model with the built-in redundancy, referred to as $Y_{red}$, can be expressed as follows.
\[ Y_{\text{red}} = Y_{\text{net}} + (1 - Y_{\text{net}}) \times \alpha_{\text{red}} \quad (4.4) \]

\[ \alpha_{\text{red}} = \sum_{i=0}^{n} \sum_{j=0}^{n} C(n, i) \times C(n, j) \times P_{\text{red}}^{n-i-j} \times P_{\text{red}} \quad (4.5) \]

\[ P_{\text{red}} = (1 - P_{i} \cdot \frac{r + \log Y}{L})^{L} \times (1 - P_{CP})^{CP} \times (1 - P_{D})^{D} \quad (4.6) \]

where,

- \( Y_{\text{net}} \): yield with no defect tolerance, i.e., the raw yield.
- \( Y_{\text{red}} \): yield with defect-tolerance of built-in redundancy.
- \( n \): number of row/column in the core array.
- \( \alpha_{\text{red}} \): rate that built-in-redundancy defect-tolerance will repair defects.
- \( P_{\text{red}} \): yield of a single NW with built in redundancy.
- \( r \): hard to mask area in built-in redundancy. (\( r = L \times 0.1 \))
- \( L \): horizontal length of a nanotile.

Figure 12. Built-in-redundancy repair of the defective area except the hard to mask area [8].
In the defect-tolerant yield model, $Y_{red}$, we consider the yield loss, i.e., $1 - Y_{net}$, as the target non-yield to improve. The defect-tolerance rate, i.e., $\alpha_{red}$, is the rate that the built in redundancy will repair. Thus, the built in redundancy can salvage a portion of the yield loss, i.e., $1 - Y_{net}$.

In the proposed yield model, $\alpha_{red}$, i.e., defect-tolerance rate, is calculated based on the information in the area such as the ratio of maskable and hard-to-mask areas. Hard-to-mask area occurs in the area where the following or next stage logic can not mask it. In other words, if the defect hits near the pull down/up without having a masking-capable AND/OR plane follow (refer to the folded line in Figure (12)), the area from $gnd$ on the right end to the first FET located in the same NW is always to be hard-to-mask. In order to calculate this area, the distance, $r$, can be calculated. As shown in Figure (12), there is no $r$ in the top NW, while there is $r$ in the second top NW in the nanotile, in which case, the hard to mask area will be $r + \log Y$. $r$ is an important element for the yield with built-in redundancy because $\log Y$ is always included in the hard to mask area. Expanding this analysis across the entire nanotile, $r$ is generally 10% of $L$ out of all NWs in a nanotile. Therefore, the yield of a single NW with the built-in redundancy, i.e., $P_{red}$, is based on the area-based probability of the hard to mask $(r + \log Y)$ area. Notice that in the non-defect tolerant case, the yield of a single NW ($P_{wire}$) is affected by the NW defects significantly with more impact especially on $P_l$, while in the built-in redundancy case, $P_{red}$ is able to achieve a better yield due to the fact that $P_l$ is decreased by the AND-OR masking of the hard to mask area. Therefore, the defect tolerance rate (i.e., $\alpha_{red}$) can be calculated for the entire NWs based on this single NW yield.
4.2.2 Interleaving Nanowires

The yield with the interleaving technique, referred to as $Y_{inter}$, can be expressed as follows.

$$Y_{inter} = Y_{net} + (1 - Y_{net}) \times \alpha_{inter} \quad (4.7)$$

$$\alpha_{inter} = \sum_{i=0}^{n} \sum_{j=0}^{n} C(n, i) \times C(n, j) \times P_{inter}^{n-i-j} \times P_{inter}^{ij} \quad (4.8)$$

$$P_{inter} = (1 - \frac{P_i}{L})^{L} \times (1 - P_{CP})^{CP} \times (1 - P_D)^{D} \quad (4.9)$$

where,

• $Y_{inter}$: yield with defect-tolerant of interleaving.

• $\alpha_{inter}$: rate interleaving defect-tolerant capability will repair defects correctly.

• $P_{inter}$: yield of single NW in interleaving technique.

Figure 13. Interleaving tolerates the defective area by exchanging two NW [13].
The interleaving can tolerate the defects when they hit on a nanotile by switching the NWs. However, it also has the **hard to mask area** when the defects hit near the pull up/down because it is impossible to switching the pull up/down NW with other normal NW. In this case, only pull up/down area will be the **hard to mask area** (refer to the folded line in Figure (13)). Taking the ratio of the defective area (i.e., \( \log Y \)) into the \( P_{\text{wire}} \), the yield of a single NW (\( P_{\text{inter}} \)) can achieve a better yield than when the built-in redundancy is employed because the decreased defect area reduces the \( P_{l} \) further.

### 4.3.3. Inserting weak pull-up/down nanowires

The yield with the inserting weak pull-up/down nanowires, referred to as \( Y_{\text{pull}} \), can be expressed as follows.

\[
Y_{\text{pull}} = Y_{\text{net}} + (1 - Y_{\text{net}}) \times \alpha_{\text{pull}} \tag{4.10}
\]

\[
\alpha_{\text{pull}} = \sum_{i=0}^{n} \sum_{j=0}^{n} C(n,i) \times C(n,j) \times P_{\text{pull}}^{n-i-j} \times P_{\text{pull}}^{ij} \tag{4.11}
\]

\[
P_{\text{pull}} = (1 - P_{l} \frac{P}{L}) \times (1 - P_{\text{CP}})^{CP} \times (1 - P_{D})^{D} \tag{4.12}
\]

where,

- \( Y_{\text{pull}} \): yield with defect-tolerant of inserting weak pull up/down NW.
- \( \alpha_{\text{pull}} \): rate inserting weak pull up/down NW capability will repair defects correctly.
- \( P_{\text{pull}} \): yield of single NW in inserting weak pull up/down NW technique.
- \( P \): length of defect area in inserting weak pull up/down NW technique. \( P = \frac{\log Y}{2} \)
The defect-tolerance rate, i.e., $\alpha_{\text{pull}}$, can salvage the yield loss, $1 - Y_{\text{net}}$.

The technique to insert weak pull-down/up NWs works by forcing the defective signal to pull up/down correctly. This technique can further tolerate the defective areas and defects that the interleaving or built in redundancy can not cover. Weak NWs can not be repaired by using the built-in redundancy as shown in Figure (13) because although after repairing the defective NW area with interleaving and built-in-redundancy, the defective area (i.e., $\log(Y)$) still exits. We can further reduce this defective length by inserting weak vertical pull-down NW forcing to pull down the defective signal 1 to 0, between OR and AND planes. Since it can repair most of the defective areas in the nanotile, it has a minimum total yield out of three techniques.

Figure 14. Inserting weak pull up/down NWs minimize the defect area[4].
CHAPTER 5

PARAMETRIC SIMULATION

Based on the yield models, extensive simulations are conducted in this chapter in order to demonstrate the validity of the proposed models and parametric-optimization of the yield.

In Figure (15), the yield in [8] is shown for their proposed defect tolerance techniques as are used as the base defect tolerance techniques in this thesis. Figure (16) shows the yields with the same defect tolerance techniques in [8] for comparison, and it shows a slight disagreement. However, the general trends of the plots in both figures are in good agreement for us to be able to use our proposed yield models as a basis for further yield optimization.

![Figure 15. Yield with combination of some techniques in [8].](image-url)
Figure 16. Applied yield modeling graph in this thesis

However, the yields in [8] are not able to provide the information how to evaluate each individual yield or any synergistic effect of the defect tolerance techniques they proposed since there is no solid theoretical derivation of the yields provided in order to adequately assess the yields in a parametric manner. In this thesis, the yield model for each defect tolerant technique is developed based on the nature of the defects involved in an area-based analysis, thereby establishing an adequate foundation to evaluate and optimize the manufacturing process and defect tolerance by providing a capability to take into account the effect of each individual defect tolerance technique or synergetic effect of various combinations of the techniques.

In this context, the effect of the defect tolerant techniques for the NASIC on WISP-0 will be studied through numerical simulation in this section. Parameters used in the 9 simulations are summarized in Table 1.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>$n$</th>
<th>$x$</th>
<th>$D$</th>
<th>$CP$</th>
</tr>
</thead>
<tbody>
<tr>
<td>value</td>
<td>$\text{var}$</td>
<td>$\text{var}$</td>
<td>2</td>
<td>$n$</td>
</tr>
</tbody>
</table>

Even if the defect rates of nano-scale fabrics will improve over time along with the defect tolerance, defect rate of nanodevices are expected to remain in the few percent range [13]. Huge nano-scale systems are generally to be defective at about 5% range. In practice as is also considered in this thesis, defect rates in the nanofabrics around 15% is considered [4], [14].

In Figure (17), the yield of a single NW with broken NW defects is shown. $P_{\text{yield}}$ with broken NWs is calculated by using Equation (4.1) and shown along with $CP$, i.e., the number of crosspoints, in the range from 10 to 150. The nanotile is assumed to have at least 10 NWs and at most 150 NWs because the number of NWs are important elements of deciding proper AND-OR logic planes. The defect rate is assumed to be 0.02 and the length of the core array is set to be 0.05. The number of crosspoints is regarded as the number of NWs in a single NW with several contact points with row/column NWs. Notice that single NW with the broken NWs is affected significantly by the number of crosspoints as shown in Figure (17), where as the yield is extended to the entire nanotiles, the yield drop is impacted by the number exponentially.
Figure 17. Yield of a single nanowire versus the number of crosspoints.

In Figure (18)-(22), the yield of three different defect tolerance techniques in NASIC is evaluated. Each Figure has four plots varying the defect tolerance techniques of non-defect-tolerant, built-in-redundancy, interleaving and inserting weak pull-up/down NW, at defect rate 0 to 0.16. Fixed length variable $x = 0.00005$ is used. $P_{CP}$ and $P_D$ are assumed to be 0 because the defects are primarily due to the defective crosspoint and decoder and again note that those defects are viewed as an failure on the length as mentioned in the previous chapter. For the nanotile with no defect tolerance such that it has a yield $> 30\%$ at a defect rate 0.02 as shown in Figure (18). In case of built-in redundancy and interleaving, the yield drops drastically down to 0 as the defect rate becomes higher than 0.04. A slight almost negligible difference can be observed in the yields between built-in redundancy and interleaving due to the smaller defect areas as the length of core array gets smaller. Notice that although each technique does improve the yield of WISP-0 under broken NWs, inserting weak pull-up/down
NWs contributes significantly to improve the yield. The yield of inserting weak pull-up/down NWs stays above 60% when the defect rate is 0.01. The yield of a nanotile can be further enhanced by manipulating the number of NWs as shown in Figure (19)-(22). The nanotile with the three defect tolerance techniques at \( n=30 \) satisfies the yield > 50% at defect rate up to 0.14. Thus, in order to meet a yield requirement > 50% at defect rate 0.14, the minimal requirements of these nanotile is to have \( n=30 \).

Figure 18. The yield of each defect tolerance technique when considering broken NWs at \( n=90 \) and \( x=0.00005 \ (5\times10^{-5}) \)
Figure 19. The yield of each defect tolerance technique when considering broken NWs at $n=150$ and $x=0.00005 \times 10^{-5}$

Figure 20. The yield of each defect tolerance technique when considering broken NWs at $n=120$ and $x=0.00005 \times 10^{-5}$
Figure 21. The yield of each defect tolerance technique when considering broken NWs at \( n=60 \) and \( x=0.00005 \ (5\times10^{-5}) \)

Figure 22. The yield of each defect tolerance technique when considering broken NWs at \( n=30 \) and \( x=0.00005 \ (5\times10^{-5}) \)
Another useful measurement of defect tolerance on NASIC is the length of core nanoarrays, in which row and column NWs are considered together. Figure (23) shows the yield along the length of the core nanoarrays of a single NW at a constant number of crosspoints. The number of NWs is assumed to be 90 and the other defect rate is 0.02. As in the case of the varying number of crosspoints, the yield with changing length of the core nanoarray a similar yield improvement.

Figure 23. Yield of a single nanowire versus the length of core nanoarray.

The yield of the non-defect tolerant and defect tolerant techniques versus various combinations of row and column length of core nanoarrays are shown in Figure (24)-(27). Three different defect tolerant techniques, that is, the built-in-redundancy, interleaving and adding pull-up/down NW at different defect rates from 0 to 0.14 are assumed at the same row and column length. Fixed number of NWs, e.g., \( n = 90 \), is assumed. In Figure (25), in case of built-in-redundancy, row length of core nanoarray
0.00005 results in a yield over 50% when the defect rate is 0.01 whereas the same number of NWs with length 0.000005 results in yield > 90% at the same defect rate as shown in Figure (27). When applying the pull-up/down-based defect tolerance technique, the yield obtained is > 99.8% at the same defect rate as in Figure (27). Therefore, the simulation results shown in Figure (24) - (27) confirm that the yield is significantly sensitive to and influenced by the length of core nanoarray. In order to meet a yield requirement >50% at defect rate up to 0.14, the required length of core nanoarray is 0.0000005 as shown in Figure (28).

Figure 24. Yield for each defect tolerance technique with broken NWs when \( n=90 \) and \( x=0.0005(5\times10^{-4}) \).
Figure 25. Yield for each defect tolerance technique with broken NWs when $n=90$ and $x=0.000005(5 \times 10^{-5})$. 

Figure 26. Yield for each defect tolerance technique with broken NWs when $n=90$ and $x=0.000005(5 \times 10^{-6})$. 

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Figure 27. Yield for each defect tolerance technique with broken NWs when \( n=90 \) and \( x=0.0000005(5\times10^{-7}) \).

Furthermore, a synergetic yield improvement can be obtained through combination of the defect tolerance techniques. In Figure (28), the yields of various combinations of the defect tolerance techniques are simulated and shown.
Figure 28. Yield of various combinations of the defect tolerance techniques when \( n=15 \) and \( x=0.05 \).

In Figures (29)-(32), various number of NWs are simulated with fixed length = 0.00005. Even the yield by inserting weak pull up/down which is the best contributor to the yield according to the analysis, would not achieve over 90%; yet the yield with all the three techniques combined achieves over 99% at defect rate = 0.02 as shown in Figure (31). Particularly, \( Y_{\text{red+inter}} \), \( Y_{\text{inter+pull}} \) and \( Y_{\text{red+inter+pull}} \) individually achieves an average yield > 95% at the same defect rate. In other words, it reveals that any technique combined with the inserting weak pull up/down NWs provides the best yield than other combinations. In Figure (29) - (32), even though the yield of \( Y_{\text{red+inter}} \) reveals a better yield than \( Y_{\text{pull}} \) in the early range, \( Y_{\text{pull}} \) sustains the yield with a smoother drop than others because it suffers least from the defective-area in the nanotile regardless of the redundancy and interleaving. In order to achieve a required
yield > 50\% up to defect rate = 0.1, the minimum requirement of the number of NWs appeared to be 30.

Figure 29. Yield of various combinations of the defect tolerance techniques when $n=120$ and $x=0.00005$.

Figure 30. Yield of various combinations of the defect tolerance techniques when $n=90$ and $x=0.00005$. 
Figure 31. Yield of various combinations of the defect tolerance techniques when $n=60$ and $x=0.00005$.

Figure 32. Yield of various combinations of the defect tolerance techniques when $n=30$ and $x=0.000005$. 
The effect of the length of the nanotile is also simulated in Figure (28) - (31). In Figure (29), the yield of $Y_{pull}$ is around 60%, while yield of the three combined technique is over 80% when defect rate = 0.02. Moreover, the yield of the three combined techniques is over 99% as the length is smaller as shown in Figure (30). In order to guarantee a yield > 50% up to defect rate = 0.1, the length of nanotile is required to be $x = 0.0000005 \times 10^{-7}$.

Figure 33. Yield of various combinations of defect tolerance techniques when $x = 0.0005 \times 10^{-4}$ and $n = 90$
Figure 34. Yield of various combinations of defect tolerance techniques when $x = 0.00005 \ (5 \times 10^{-5})$ and $n = 90$

Figure 35. Yield of various combinations of defect tolerance techniques when $x = 0.000005 \ (5 \times 10^{-6})$ and $n = 90$
Figure 36. Yield of various combinations of defect tolerance techniques when $x = 0.0000005 \times 10^{-7}$ and $n = 90$

Based on the extensive and various simulations, the top three combinations of the defect tolerance techniques with respect to their yield are $Y_{\text{red+pull}}$, $Y_{\text{inter+pull}}$, and $Y_{\text{red+inter+pull}}$. In order to have these three combinations to achieve a yield $> 99.8\%$ in Figure (37), an optimal and reliable circuit can be realized, and the optimal requirements in the simulations are summarized in Table 2.

Table 2. Minimum Requirements

<table>
<thead>
<tr>
<th>Number of NWs</th>
<th>Length of core nano array</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>0.000034</td>
</tr>
<tr>
<td>30</td>
<td>0.000002</td>
</tr>
<tr>
<td>60</td>
<td>0.00000013</td>
</tr>
<tr>
<td>90</td>
<td>0.000000025</td>
</tr>
<tr>
<td>120</td>
<td>0.000000008</td>
</tr>
<tr>
<td>150</td>
<td>0.000000003</td>
</tr>
</tbody>
</table>
Figure 37. Minimum requirement on the number of NWs and the length of core nanoarray to achieve yield $> 99.8\%$.
CHAPTER 6

CONCLUSION

Advances in nano-scale devices including semiconductor nanowires (NW) and NW crossbars have made possible the building of the nano-scale computing systems. Yield and data integrity are the most emphasized requirements of nano-scale computing system, because defects and faults due to harsh environment in nano manufacturing environment can be experienced throughout the process. A yield modeling, assurance and optimization method for the defect tolerant NASIC system under broken NW defects has been proposed and validated through extensive parametric simulations in this thesis. Ultimately, intelligent exploitation of the proposed yield modeling and simulation methods will make possible to realize a reliable NASIC-based computing system. According to the simulation results given in this thesis, the defect tolerant NASIC system with 15 row and column NWs, respectively, each with length $= 0.000034$ on horizontal and vertical core nanoarray in a nanotile can achieve a yield higher than 99.8%.
REFERENCES


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Scope and Method of Study: Reliability and data integrity are the commonly emphasized requirements of nanoscale computing system, because faults due to harsh environment in nano area, can be experienced throughout the process. Acceptable dependability for these system have been achieved by conventional CMOS designs and manufacturing methods using redundancy and repair. Even if reconfiguration (repair) of nanoscale array designs using redundancy is the most common technique for enhancement of reliability with faults, unfortunately, it is not directly applicable in nanoscale systems because they have been designed for very small defect rates. Instead of reconfiguration, some defect tolerant techniques are introduced for nanoscale application-specific architecture, called NASIC, which is based on semiconductor NW grids and FETs at crosspoints.

Findings and Conclusions: This paper initially investigates a defect model under broken NW to establish a reliable foundation of architecture on 2-D semiconductor NW arrays. Then, dependability of NASIC with three different defect tolerant techniques, which is built-in-redundancy, interleaving and adding weak pull-up/down NW, is measured in terms of reliability (i.e., the probability that the system performs correctly). Finally, optimal defect tolerant technique for the fault-tolerant system is proposed and verified through a series of parametric simulations. Thereby, design and fabrication of effective and highly reliable fault-tolerant system can be realized for dependable nanoscale architecture.